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| Faculty of engineering, cairo university, computer engineering department |
| Architecture Project |
| Simple PDP-11 |
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Memory Access Analysis

Group 1: Two Operands Regular Instructions (ADD, ADC, SUB, SUBC, AND, OR, XNOR):  
Addressing modes are (RGS: register, IND\_RGS: indirect register)

|  |  |  |
| --- | --- | --- |
| SRC | DST | MA |
| RGS | RGS | 1 |
| RGS | IND\_RGS | 3 |
| RGS | Autoincremet | 3 |
| RGS | IND\_autoincremetn | 4 |
| RGS | Autodecrement | 3 |
| RGS | IND\_Autodec | 4 |
| RGS | Indexed | 4 |
| RGS | Ind\_Indexed | 5 |

|  |  |  |
| --- | --- | --- |
| SRC | DST | MA |
| IND\_RGS | RGS | 2 |
| IND\_RGS | IND\_RGS | 4 |
| IND\_RGS | Autoincremet | 4 |
| IND\_RGS | IND\_autoincremetn | 5 |
| IND\_RGS | Autodecrement | 4 |
| IND\_RGS | IND\_Autodec | 5 |
| IND\_RGS | Indexed | 5 |
| IND\_RGS | Ind\_Indexed | 6 |

|  |  |  |
| --- | --- | --- |
| INC | RGS | 2 |
| INC | IND\_RGS | 4 |
| INC | Autoincremet | 4 |
| INC | IND\_autoincremetn | 5 |
| INC | Autodecrement | 4 |
| INC | IND\_Autodec | 5 |
| INC | Indexed | 5 |
| INC | Ind\_Indexed | 6 |

|  |  |  |
| --- | --- | --- |
| IND\_INC | RGS | 3 |
| IND\_INC | IND\_RGS | 5 |
| IND\_INC | Autoincremet | 5 |
| IND\_INC | IND\_autoincremetn | 6 |
| IND\_INC | Autodecrement | 5 |
| IND\_INC | IND\_Autodec | 6 |
| IND\_INC | Indexed | 6 |
| IND\_INC | Ind\_Indexed | 7 |

|  |  |  |
| --- | --- | --- |
| DEC | RGS | 2 |
| DEC | IND\_RGS | 4 |
| DEC | Autoincremet | 4 |
| DEC | IND\_autoincremetn | 5 |
| DEC | Autodecrement | 4 |
| DEC | IND\_Autodec | 5 |
| DEC | Indexed | 5 |
| DEC | Ind\_Indexed | 6 |

|  |  |  |
| --- | --- | --- |
| IND\_DEC | RGS | 3 |
| IND\_DEC | IND\_RGS | 5 |
| IND\_DEC | Autoincremet | 5 |
| IND\_DEC | IND\_autoincremetn | 6 |
| IND\_DEC | Autodecrement | 5 |
| IND\_DEC | IND\_Autodec | 6 |
| IND\_DEC | Indexed | 6 |
| IND\_DEC | Ind\_Indexed | 7 |
| IND\_INDEX | RGS | 4 |
| IND\_INDEX | IND\_RGS | 6 |
| IND\_ INDEX | Autoincremet | 6 |
| IND\_ INDEX | IND\_autoincremetn | 7 |
| IND\_ INDEX | Autodecrement | 6 |
| IND\_ INDEX | IND\_Autodec | 7 |
| IND\_ INDEX | Indexed | 7 |
| IND\_ INDEX | Ind\_Indexed | 8 |

|  |  |  |
| --- | --- | --- |
| INDEX | RGS | 3 |
| INDEX | IND\_RGS | 5 |
| INDEX | Autoincremet | 5 |
| INDEX | IND\_autoincremetn | 6 |
| INDEX | Autodecrement | 5 |
| INDEX | IND\_Autodec | 6 |
| INDEX | Indexed | 6 |
| INDEX | Ind\_Indexed | 7 |

Group 2: Two Operands Special Instructions (MOV, CMP):  
As MOV doesn’t require the final data of the destination, just the address, and CMP doesn’t store the final value of the operation.

So, the second table would differ from the previous one, as MA would be less by 1, except when RGS is at the destination.

|  |  |  |
| --- | --- | --- |
| SRC | DST | MA |
| RGS | RGS | **1** |
| RGS | IND\_RGS | 2 |
| RGS | Autoincremet | 2 |
| RGS | IND\_autoincremetn | 3 |
| RGS | Autodecrement | 2 |
| RGS | IND\_Autodec | 3 |
| RGS | Indexed | 3 |
| RGS | Ind\_Indexed | 4 |

|  |  |  |
| --- | --- | --- |
| SRC | DST | MA |
| IND\_RGS | RGS | **2** |
| IND\_RGS | IND\_RGS | 3 |
| IND\_RGS | Autoincremet | 3 |
| IND\_RGS | IND\_autoincremetn | 4 |
| IND\_RGS | Autodecrement | 3 |
| IND\_RGS | IND\_Autodec | 4 |
| IND\_RGS | Indexed | 4 |
| IND\_RGS | Ind\_Indexed | 5 |

|  |  |  |
| --- | --- | --- |
| INC | RGS | **2** |
| INC | IND\_RGS | 3 |
| INC | Autoincremet | 3 |
| INC | IND\_autoincremetn | 4 |
| INC | Autodecrement | 3 |
| INC | IND\_Autodec | 4 |
| INC | Indexed | 4 |
| INC | Ind\_Indexed | 5 |

|  |  |  |
| --- | --- | --- |
| IND\_INC | RGS | **3** |
| IND\_INC | IND\_RGS | 4 |
| IND\_INC | Autoincremet | 4 |
| IND\_INC | IND\_autoincremetn | 5 |
| IND\_INC | Autodecrement | 4 |
| IND\_INC | IND\_Autodec | 5 |
| IND\_INC | Indexed | 5 |
| IND\_INC | Ind\_Indexed | 6 |

|  |  |  |
| --- | --- | --- |
| DEC | RGS | **2** |
| DEC | IND\_RGS | 3 |
| DEC | Autoincremet | 3 |
| DEC | IND\_autoincremetn | 4 |
| DEC | Autodecrement | 3 |
| DEC | IND\_Autodec | 4 |
| DEC | Indexed | 4 |
| DEC | Ind\_Indexed | 5 |

|  |  |  |
| --- | --- | --- |
| IND\_DEC | RGS | **3** |
| IND\_DEC | IND\_RGS | 4 |
| IND\_DEC | Autoincremet | 4 |
| IND\_DEC | IND\_autoincremetn | 5 |
| IND\_DEC | Autodecrement | 4 |
| IND\_DEC | IND\_Autodec | 5 |
| IND\_DEC | Indexed | 5 |
| IND\_DEC | Ind\_Indexed | 6 |
| IND\_INDEX | RGS | **4** |
| IND\_INDEX | IND\_RGS | 5 |
| IND\_ INDEX | Autoincremet | 5 |
| IND\_ INDEX | IND\_autoincremetn | 6 |
| IND\_ INDEX | Autodecrement | 5 |
| IND\_ INDEX | IND\_Autodec | 6 |
| IND\_ INDEX | Indexed | 6 |
| IND\_ INDEX | Ind\_Indexed | 7 |

|  |  |  |
| --- | --- | --- |
| INDEX | RGS | **3** |
| INDEX | IND\_RGS | 4 |
| INDEX | Autoincremet | 4 |
| INDEX | IND\_autoincremetn | 5 |
| INDEX | Autodecrement | 4 |
| INDEX | IND\_Autodec | 5 |
| INDEX | Indexed | 5 |
| INDEX | Ind\_Indexed | 6 |

Group3: One Operand Instructions (INC, DEC, CLR, INV, LSR, ROR, RRC, ASR, LSL, ROL, RLC):

|  |  |
| --- | --- |
| **Destination** | **MA** |
| Register | **1** |
| Indirect Register | 3 |
| Autoincremet | 3 |
| Indirect Autoincremetn | 4 |
| Autodecrement | 3 |
| Indirect Autodecrement | 4 |
| Indexed | 4 |
| Indirect Indexed | 5 |

Group 4: Jumpers and Stackers (JSR, RTS, ITR, IRET):

|  |  |
| --- | --- |
| Operation | Memory Access |
| JSR | 3 |
| RTS | 2 |
| ITR | 3 |
| IRET | 3 |

Group 5: Branches, HLT and NO Operation:

Memory Access = 1 for fetching any of these instructions, no memory accessing is required for any of them.

# Architecture:

#of Registers = 8 (including stack register and program counter)

#of added TEMP registers = 3 (SOURCE, Y, Z)  
 SOURCE: is for **storing** the source value for two operand instructions  
 Y: is for adding **offsets** to the indexed modes  
 Z: is for **buffering** the ALU output

#of special registers = **4**(MAR, MDR, IR, FLAG)

#of Busses = 1

